WHAT IS CLAIMED IS:

1. A system for controlling the number of iterations to be performed by an iterative decoder, comprising:

an input port configured to receive a data throughput value;

a processor configured to determine an efficient number of iterations for an iterative decoder based on the data throughput value; and

an output port configured to provide the efficient number of iterations based on the determination by the processor.

2. The system of claim 1, wherein the data throughput value is the number of packets that are currently stored in a data packet queue.

3. The system of claim 1, wherein the data throughput value is the rate at which data packets are being received by a receiving module include the system for controlling the number of iterations to be performed by an iterative decoder.

4. The system of claim 2, wherein the determination by the processor is made by referencing a table.

5. The system of claim 4, wherein the table includes a number of iterations to be performed by the iterative decoder for each possible length of the packet data queue.

6. The system of claim 1, wherein the processor is further configured to calculate a number of iterations to be performed by the iterative decoder using the data throughput value as an input value.

7. A method for real-time optimization of error detection and correction algorithms, comprising:

receiving a data throughput value;

determining a number of iterations to be performed by an iterative decoder based on the data throughput value; and

providing the number of iterations to be performed to the iterative decoder.

8. The method of claim 7, wherein the data throughput value is the number of packets that are currently stored in a data packet queue.

9. The method of claim 7, wherein the data throughput value is the rate at which data packets are being received by a receiving module.

10. The method of claim 7, wherein determining a number of iteration to be performed includes referencing a table.

11. The method of claim 10, wherein the table includes a number of iterations to be performed by the iterative decoder for each possible length of the packet data queue.

12. The method of claim 7, wherein the determination by the processor is made based on a calculation using the data throughput value as an input value.

13. A modem for a wireless communication system, comprising:

a data packet queue configured to store data packets received as input to the modem;

an iterative decoder configured to decode data packets stored in the data packet queue; and

a processor configured to determine a data throughput value and determine the number of iterations to be performed by the iterative decoder based on the data throughput value and further configured to control the number of iterations performed by the iterative decoder based on the determination.

14. The modem of claim 13, wherein the processor is configured to determine the number of iterations to be performed each time before the iterative decoder begins to decode a packet.

15. The modem of claim 13, wherein the processor is configured to determine the number of iterations to be performed each time before the iterative decoder begins an iteration while decoding a packet.

16. The system of claim 13, wherein the data throughput value is the number of packets that are currently stored in a data packet queue.

17. The modem of claim 13, wherein the data throughput value is the rate at which data packets are being received by a receiving module include the system for controlling the number of iterations to be performed by an iterative decoder.

18. The modem of claim 13, wherein the determination by the processor is made by referencing a table.

19. The method of claim 18, wherein the table includes a number of iterations to be performed by the iterative decoder for each possible length of the packet data queue.

20. The modem of claim 13, wherein the determination by the processor is made based on a calculation using the data throughput value as an input value.